## REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 1-9, 13-16 and 20-27 are present in this application. Claims 3-9 are withdrawn. Amended claims 1, 15 and 27 are supported by Fig. 1. No new matter is believed to be added.

Claims 1, 2, 13-16, 20-25 and 27 are rejected under 35 U.S.C. § 102(b) over U.S. 6,400,471 (Kuo et al.). Claim 26 is rejected under 35 U.S.C. § 103(a) over Kuo et al. in view of US 6,002,446 (Eglit).

The image processing apparatus of claims 1, 15 and 27 includes a buffer memory for image data storage and a compression unit for generated compressed image data. The compressed image data is output directly from the compression unit to a data bus connected to a storage unit and to the compression unit for storing the compressed image data (claims 1 and 15), or a DMA controller controls transfer of the compressed image data between the compression unit and the storage unit, and the compressed image data is output directly from the compression unit, which is connected to the bus, via the bus to the storage unit (claim 27). In claim 1, an input of said buffer memory is connected, separate from said bus, only to said image processing unit to receive only said image data from said image processing unit, and an output of said buffer memory is connected, separate from said bus, only to said compression unit to output said image data only to said compression unit. The separate connection provides for reduced transfers between the storage unit and the image processing part.

Turning to the § 102(b) rejection, Kuo et al. discloses in Figure 11 an architecture having a line reader 620, DSP 922, JPEG hardware 924 and line writer 650. The architecture is associated with a data structure having a plurality of buffers 1110, 1120, 1130, and 1140. The Office Action, in paragraph 4, identifies buffer 1140 as the storage unit and line reader

620, DSP 922, ping pong buffers 1130, JPEG hardware 924 and line writer 650 as image processing part. Data is transferred between the buffers in the memory structure and elements 620, 922, 924 and 650. The Office Action does not particularly identify the bus. The Office Action generally describes that "data are transferred across a bus for hardware" and the JPEG hardware 924 is "hardware." JPEG hardware 924 transfers data to the JPEG hardware 924 "via a bus." The Office Action does not describe in any detail what constitutes the bus, and Fig. 11 of Kuo et al. only shows schematic connections between the elements shown.

In claim 1 the compression unit is connected to the storage unit and the storage unit is connected to the image processing part via the bus. The buffer memory is connected to the compression unit and the image processing unit separate from the bus. Kuo et al does not disclose the bus and the connections separate from the bus recited in claim 1. Kuo et al. makes no distinction between the connections of the elements of Fig. 11 as all are shown the same. Also, the general mention of a bus is insufficient to disclose the connections using and separate from the bus recited in claim 1. Claim 1 is not disclosed by Kuo et al.

Claim 15 recites the compression unit being connected to the storage unit and the storage unit being connected to the image processing part via the bus. Claim 15 also recites inputs of the first and second buffer memories being connected, separate from said bus, only to said image processing unit and outputs of said first and second buffer memories are connected, separate from said bus, only to said compression unit. Kuo et al does not disclose the bus and the connections separate from the bus recited in claim 15. Kuo et al. makes no distinction between the connections of the elements of Fig. 11 as all are shown the same. Also, the general mention of a bus is insufficient to disclose the connections using and separate from the bus recited in claim 15. Claim 15 is also not disclosed by Kuo et al.

Claim 27 recites the compression unit being connected to the storage unit and the storage unit being connected to the image processing part via the bus. Claim 27 also recites an input of said buffer memory is connected, separate from said bus, only to said image processing unit, to receive only said image data from said image processing unit, and an output of said buffer memory is connected, separate from said bus, only to said compression unit. Kuo et al does not disclose the bus and the connections separate from the bus recited in claim 27. Kuo et al. makes no distinction between the connections of the elements of Fig. 11 as all are shown the same. Also, the general mention of a bus is insufficient to disclose the connections using and separate from the bus recited in claim 27. Claim 27 is also not disclosed by Kuo et al.

Eglit is cited for ping-pong buffers with a line width being greater than the line width of the memory. Even if such ping-pong buffers are included in the architectures of Kuo et al., the deficiencies noted above in Kuo et al. remain. The apparatuses of claims 1, 15 and 27 are neither taught nor suggested by a combination of Kuo et al. and Eglit.

It is respectfully submitted the present application is in condition for allowance, and a favorable action to that effect is respectfully requested.

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